ECSI Fibrotools — SK Hynix CET Co-Development Strategy

Complete Internal Playbook

Prepared for: ECSI Fibrotools, Inc. | Dr. Igor V. Kadija, Founder & CEO **Prepared by:** Contract Advisor — MEMS, Microelectronics & Semiconductor Strategy **Date:** July 2026 **Classification:** CONFIDENTIAL — Internal Use Only

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PART 1: EXECUTIVE OVERVIEW

The Situation in Plain Terms

CET (Contact Electroplating Technology) is a patented, physics-breaking innovation at the prototype stage. It is currently a handheld device — not a lab-ready or production-ready tool. A recent test deposited 100 microns of platinum where 5–7 microns were intended. The fundamental electrochemical mechanism is extraordinarily powerful; what is missing is the precision mechatronics, automation, and control systems required to harness it at semiconductor scale.

We are not selling SK Hynix a tool. We are offering them the exclusive opportunity to co-fund and co-develop the final phase of a patented breakthrough — and in exchange, they get a competitive weapon that Samsung and Micron cannot buy.

Why SK Hynix Specifically

SK Hynix is investing **$3.87 billion** in a new advanced packaging R&D and fabrication facility at the **Purdue Research Park in West Lafayette, Indiana** — targeting HBM5 and next-generation 3D DRAM production by 2028. Their entire roadmap depends on solving the exact problem CET addresses: void-free, ultra-uniform copper filling in high-aspect-ratio Through-Silicon Vias (TSVs) and microbumps. They also operate a formal **Open Research Platform** actively seeking U.S.-based innovation partners, and they recently signed a $5 billion co-innovation agreement with Applied Materials — proving they are willing to fund external technology development at scale.

The Warm Introduction Advantage

A repeat ECSI customer at Purdue University has recommended SK Hynix as a target and can make a direct introduction. In Korean corporate culture, a trusted academic referral is not a convenience — it is the difference between a meeting and a deleted email. This asset must be activated immediately and used correctly.

The Core Narrative

> *"Dr. Kadija has patented a fundamental breakthrough in electroplating physics that eliminates the boundary layer and edge effect problems that plague TSV and microbump plating. The physics work — in fact, the deposition engine is so powerful it recently over-plated 100µm of platinum in a test designed for 5µm. What we lack is the precision mechatronics and control systems that SK Hynix possesses. We're not here to sell you a finished tool. We're here to propose an incubation partnership: you provide the engineering muscle and funding, we provide the patents and electrochemical expertise, and SK Hynix secures exclusive rights to a technology that could permanently separate you from Samsung and Micron."*

PART 2: THE 4-PHASE ENGAGEMENT ROADMAP

Phase 01 — Activate the Warm Introduction (Weeks 1–4)

Objective: Convert the Purdue referral into a credible, correctly framed first contact with the right SK Hynix technical personnel.

Step 1 — Brief the Purdue Champion Schedule a call with the Purdue contact. Fully brief them on CET's current stage — including the prototype limitations and the 100µm setback. Do not ask them to oversell. Ask them to frame ECSI as "a small, highly specialized company with a novel, patented electroplating mechanism at the prototype stage, seeking an R&D incubation partner — not selling a finished product." This sets honest expectations from day one and protects the relationship.

Step 2 — Prepare the Technology Vision Brief Draft a 2-page document titled "CET for Advanced HBM Packaging: A Co-Development Proposal." It must look like an academic white paper, not a product brochure. Write in SK Hynix's language: TSV aspect ratios, microbump

pitch, HBM stack height, yield improvement, cost reduction. Include a clear diagram of the CET sandwich structure and a one-paragraph honest statement of current development stage.

Step 3 — Frame the Introduction Correctly Instruct the Purdue champion to identify the specific SK Hynix R&D engineers and process integration leads at the West Lafayette facility who work on TSV and advanced packaging. These are the right first contacts — not business development or procurement.

Step 4 — Research the West Lafayette Team Identify specific engineers via LinkedIn, conference proceedings (ECTC, IMAPS, IEEE VLSI), and Purdue's semiconductor faculty directory. Know their names, their published work, and their specific process challenges before the first meeting.

Phase 02 — First Contact & The "No-Risk" Hook (Weeks 5–10)

Objective: Secure a 45-minute technical meeting and propose a zero-cost proof-of-concept test.

Step 1 — The Facilitated Introduction Email Have the Purdue contact make a direct email introduction to the relevant SK Hynix technical lead, copying Dr. Kadija. The email should frame ECSI as a company with a novel electroplating mechanism relevant to advanced packaging challenges. Attach the 2-page Technology Vision Brief.

Step 2 — The 45-Minute Technical Meeting The agenda: (1) 15 minutes on the physics of CET — the boundary layer elimination mechanism; (2) 15 minutes on benchtop proof-of-concept data, including the 100µm over-plating incident framed as evidence of raw power; (3) 15 minutes on the co-development proposal.

Step 3 — The "No-Risk" Offer The single most powerful offer in the meeting: *"Give us one of your test wafers with your most challenging TSV structures. We will attempt to fill them with our current prototype at no cost to you. The goal is not perfect uniformity — the goal is to prove the mechanism works on your geometry. You have nothing to lose."* This removes the barrier to engagement entirely.

Step 4 — The NDA Before any wafer exchange or detailed IP discussion, execute a mutual NDA. Have a template ready before the first meeting.

Phase 03 — Proof of Concept & JDA Proposal (Weeks 11–24)

Objective: Demonstrate the CET mechanism on SK Hynix test structures and convert the relationship into a funded Joint Development Agreement.

Step 1 — Execute the Feasibility Test Use the current CET prototype on the SK Hynix test wafers. Document everything meticulously — SEM cross-sections, void analysis, deposition rate, uniformity data. Even imperfect results are valuable if they show the mechanism is working.

Step 2 — Present the Data Honestly Present the results in a follow-up meeting. Lead with what worked. Explain what the data tells you about what precision control improvements are needed. Show a clear engineering roadmap from the current prototype to a 300mm-capable Alpha tool.

Step 3 — Propose the JDA Structure: SK Hynix provides milestone-based funding ($1M–$3M) and access to their metrology and precision engineering teams. ECSI provides the CET patents, electrochemical expertise, and Dr. Kadija's time. Propose hosting the joint development work at Purdue's Birck Nanotechnology Center — a neutral, world-class cleanroom that SK Hynix already knows and trusts.

Phase 04 — Pilot Integration & Commercialization (Months 7–24+)

Objective: Build the Alpha CET tool, prove it at 300mm wafer scale, and transition to a commercial exclusivity agreement.

The Alpha tool development is funded by SK Hynix and executed jointly at Birck Nanotechnology Center. Upon successful demonstration, the partnership transitions to a formal commercialization agreement. SK Hynix selects their preferred exclusivity structure (see Part 4 of this document). If SK Hynix chooses to involve an equipment vendor (Lam Research, Applied Materials), ECSI negotiates a royalty-per-tool or royalty-per-wafer structure.

PART 3: 8 RELATIONSHIP-BUILDING PATHWAYS

Beyond the warm Purdue introduction, there are seven additional channels for building a relationship with SK Hynix. These can be pursued in parallel to accelerate engagement or used as fallback paths if the primary route stalls.

#	Pathway	Category	Difficulty	Speed
01	The Warm Introduction via Purdue University	Primary	Low	Fastest
02	SK Hynix Open Research Platform	Formal Program	Medium	Moderate
03	Conference & Publication Strategy	Industry Events	Medium	Slow (6–12 mo.)
04	Semiconductor Research Corporation (SRC)	Ecosystem	Medium	Moderate
05	Equipment Vendor Partnership (Lam / AMAT)	Strategic	High	Slow (12–18 mo.)
06	CHIPS Act & Government Co-Funding	Government	Medium	Moderate
07	Purdue Birck Nanotechnology Center	Academic	Low	Fast
08	SK Hynix Startup Investment & Seeding Program	Long Game	Medium	Moderate

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Pathway 01 — The Warm Introduction via Purdue University

Category: Primary | **Difficulty:** Low | **Speed:** Fastest

The single most valuable asset in this engagement. A trusted academic referral from a repeat ECSI customer who works directly with SK Hynix's West Lafayette team changes everything. Korean corporate culture places enormous weight on trust and long-term relationships. A cold outreach to a company of SK Hynix's scale would face enormous institutional barriers. The Purdue contact changes this entirely.

Action Items:

- Brief the Purdue contact fully and honestly on CET's current stage (prototype, not finished tool)
- Provide them with the 2-page Technology Vision Brief to share informally

- Ask them to identify the specific SK Hynix R&D engineers at the West Lafayette facility who work on TSV and advanced packaging
- Ask them to make a direct email introduction, copying Dr. Kadija

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Pathway 02 — SK Hynix Open Research Platform (Global R&D24)

Category: Formal Program | **Difficulty:** Medium | **Speed:** Moderate

SK Hynix operates a formal program called the **Open Research Platform** (part of their "Global R&D24" initiative) that explicitly invites external researchers, startups, and equipment companies to propose collaborative R&D projects. This is a structured, institutional channel that runs parallel to the warm introduction.

Action Items:

- Visit research.skhynix.com/open_research_platform and submit a formal research collaboration proposal
- Frame the proposal as a "Feasibility Study for CET-Based TSV Filling in Advanced HBM Packaging"
- Reference the Purdue connection in the proposal to add credibility
- The formal submission creates a paper trail and a second point of contact inside SK Hynix's R&D organization

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Pathway 03 — Conference & Publication Strategy

Category: Industry Events | **Difficulty:** Medium | **Speed:** Slow (6–12 months)

The semiconductor industry runs on peer-reviewed credibility. Publishing CET results in the right venues and presenting at the right conferences builds the technical reputation that makes SK Hynix engineers want to seek ECSI out — rather than the other way around.

Key Target Venues:

- **ECTC** (Electronic Components and Technology Conference) — the premier advanced packaging conference; SK Hynix engineers attend every year
- **IMAPS** (International Microelectronics Assembly and Packaging Society) — strong TSV and advanced packaging community

- **IEEE VLSI Technology Symposium** — where SK Hynix presents their own roadmap papers
- **ECS (Electrochemical Society) Meetings** — the natural home for CET's fundamental electrochemistry

Action Items:

- Submit a paper to ECTC or IMAPS on the fundamental physics of CET and benchtop proof-of-concept results
- Attend ECTC and IMAPS; identify and introduce yourself to SK Hynix process engineers in the hallways
- A published paper gives the Purdue contact something concrete to share with SK Hynix engineers

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Pathway 04 — Semiconductor Research Corporation (SRC)

Category: Ecosystem | **Difficulty:** Medium | **Speed:** Moderate

The SRC is a consortium of semiconductor companies (including SK Hynix) that co-fund pre-competitive university research. Purdue University is an SRC member institution. Proposing a CET research project through the SRC framework gives SK Hynix a low-risk, consortium-funded way to evaluate the technology without committing to a bilateral JDA immediately.

Action Items:

- Contact the SRC program manager for advanced packaging (src.org)
- Propose a university research project on "CET for High-Aspect-Ratio TSV Filling" hosted at Purdue's Birck Nanotechnology Center
- SK Hynix, as an SRC member, can co-sponsor the project and assign an internal liaison engineer — creating a formal technical relationship

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Pathway 05 — Equipment Vendor Partnership (Lam Research / Applied Materials)

Category: Strategic | **Difficulty:** High | **Speed:** Slow (12–18 months)

SK Hynix recently signed a **$5 billion co-innovation agreement with Applied Materials** at their new EPIC Center in Silicon Valley. Applied Materials and Lam Research are SK Hynix's most trusted equipment partners. If either of these companies validates CET and expresses

interest in licensing it, SK Hynix will take notice immediately. This is a longer, harder path — but it could bypass the need for a direct SK Hynix relationship entirely.

Action Items:

- Identify the Advanced Packaging or Electrochemical Deposition (ECD) product managers at Applied Materials and Lam Research
- Approach them with a technology licensing proposal: ECSI licenses the CET patents, the equipment vendor builds the production tool, and ECSI receives a royalty per tool sold
- If Applied Materials validates CET at the EPIC Center, SK Hynix will hear about it through their existing partnership

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Pathway 06 — CHIPS Act & Government Co-Funding

Category: Government | **Difficulty:** Medium | **Speed:** Moderate

The U.S. CHIPS and Science Act provides funding for domestic semiconductor R&D. SK Hynix's West Lafayette facility was established partly under CHIPS Act incentives. A joint ECSI–SK Hynix proposal for a CHIPS Act R&D grant (through NIST or NSF) would give SK Hynix a government-subsidized reason to engage with ECSI — reducing their financial risk and aligning with their existing federal commitments.

Action Items:

- Research NIST's "CHIPS R&D" programs (nist.gov/chips) for applicable grant categories
- Consult with Purdue's Office of Technology Commercialization about joint grant applications
- A government co-funding structure can reduce SK Hynix's JDA commitment from $3Mto$1M, making the ask significantly easier

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Pathway 07 — Purdue Birck Nanotechnology Center as Neutral Ground

Category: Academic | **Difficulty:** Low | **Speed:** Fast

Purdue's Birck Nanotechnology Center is a world-class cleanroom facility that SK Hynix already uses and trusts for collaborative R&D. Proposing to host all CET development work at Birck — rather than at ECSI's facility — removes a major psychological barrier for SK Hynix. It signals that ECSI is serious, has access to credible infrastructure, and is not asking SK Hynix to take a leap of faith on an unknown small company.

Action Items:

- Contact Birck’s industry partnership office to understand the process for hosting a joint industry R&D project
- Propose to the Purdue contact that the first CET feasibility test be conducted at Birck, using their metrology equipment
- Frame Birck as the “home base” for the entire co-development program in all SK Hynix communications

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Pathway 08 — SK Hynix Startup Investment & Seeding Program

Category: Long Game | **Difficulty:** Medium | **Speed:** Moderate

SK Hynix operates a startup seeding and investment arm that looks for early-stage technology companies in the semiconductor ecosystem. This is a longer-term pathway — but if the JDA route stalls, approaching SK Hynix’s investment arm (rather than their R&D organization) with a seed investment proposal is a viable alternative. A seed investment gives SK Hynix an equity stake in ECSI in exchange for funding CET development, with options to acquire exclusive rights later.

Action Items:

- Research SK Hynix’s corporate venture and investment programs
- Prepare a brief investor deck (separate from the technical brief) positioning ECSI as an early-stage deep-tech company with a patented breakthrough in electroplating
- This pathway can run in parallel with the JDA route — different decision-makers, different incentives

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PART 4: DEAL STRUCTURE OPTIONS

Full exclusivity is just one of seven ways to structure a commercial relationship with SK Hynix. Each option balances ECSI’s need to protect its IP and future markets against SK Hynix’s need for competitive advantage. These structures can also be combined.

Option	Structure	ECSI Risk	SK Hynix Appeal
A	Full Exclusivity — Memory & Advanced Packaging	High	Very High
B	Application-Specific Exclusivity	Low	High
C	Material-Specific Exclusivity	Low	Medium
D	Time-Bound First-to-Market Exclusivity	Medium	High
E	IP Split — Core vs. Joint Development IP	Low	High
F	Equipment Vendor License (Lam / Applied Materials)	Medium	Medium
G	Strategic Seed Investment	Medium	Medium

Option A — Full Exclusivity: Memory & Advanced Packaging

ECSI Risk: High | SK Hynix Appeal: Very High *Ideal for: If SK Hynix wants the broadest possible competitive moat*

SK Hynix receives exclusive rights to use CET for all memory and advanced packaging applications globally for a defined period (e.g., 5 years). ECSI retains rights for all other industries (aerospace, medical, PCB, etc.).

This is the maximum value proposition for SK Hynix — no competitor (Samsung, Micron) can access CET for memory applications during the exclusivity window. In exchange, SK Hynix pays a premium for the JDA and commits to a minimum commercialization timeline. After the exclusivity period, ECSI regains the right to license to the broader market, but SK Hynix retains a royalty-free perpetual license for their own internal use.

Advantages: Maximum competitive advantage for SK Hynix; strongest incentive to fund development; simplest deal structure to negotiate; highest upfront JDA funding potential ($3M–$10M range).

Considerations: ECSI gives up the ability to sell to Samsung, Micron, or TSMC during the exclusivity window. If SK Hynix deprioritizes CET internally, ECSI has no other revenue path during that period.

Option B — Application-Specific Exclusivity

ECSI Risk: Low | SK Hynix Appeal: High *Ideal for: Protecting ECSI's other markets while still giving SK Hynix a strong competitive advantage*

SK Hynix only cares about memory and advanced packaging. ECSI grants them exclusivity for specific applications while retaining the rights to sell or license CET for all other uses.

- **Exclusive Rights For SK Hynix:** High-Bandwidth Memory (HBM), Through-Silicon Via (TSV) filling, memory-related microbump formation, and 3D NAND stacking interconnects.
- **ECSI Retains Rights For:** Aerospace components, medical devices (implants), printed circuit boards (PCBs), flexible electronics, non-memory logic chips (CPUs, GPUs), MEMS devices, and sensor fabrication.

Advantages: ECSI retains a large addressable market. SK Hynix still gets exclusivity in the market they care about. Lower risk for ECSI if the SK Hynix relationship underperforms.

Considerations: Requires clear contractual definitions of "memory" and "advanced packaging" to prevent scope disputes. SK Hynix may push to broaden the exclusivity scope during negotiation.

Option C — Material-Specific Exclusivity

ECSI Risk: Low | SK Hynix Appeal: Medium *Ideal for: If SK Hynix's primary bottleneck is copper TSV filling specifically*

If SK Hynix's primary bottleneck is copper, the deal can be structured around the metal rather than the application.

- **Exclusive Rights For SK Hynix:** Copper (Cu) electroplating using CET for all semiconductor applications.
- **ECSI Retains Rights For:** Platinum (Pt), Gold (Au), Nickel (Ni), Ruthenium (Ru), Cobalt (Co), and specialized alloys for all industries, including semiconductor.

This is a highly favorable structure for ECSI because copper is the primary metal of interest for SK Hynix's TSV and microbump applications, while ECSI's other CET work (e.g., platinum for medical, gold for aerospace) remains completely free.

Advantages: Very clean contractual scope. ECSI retains rights to all non-copper applications. Particularly valuable if ECSI has other metal-specific applications in development.

Considerations: SK Hynix may view this as too narrow. Future memory technologies may shift to non-copper metals (e.g., ruthenium for sub-2nm barriers), requiring renegotiation.

Option D — Time-Bound First-to-Market Exclusivity

ECSI Risk: Medium | SK Hynix Appeal: High *Ideal for: SK Hynix wants a head start to beat Samsung and Micron, not permanent control*

SK Hynix funds the development and gets 100% exclusive use of the resulting CET tools for a defined period (3–5 years) after the first production tool comes online. After the exclusivity window closes, ECSI regains the full right to license or sell the technology to the broader market. SK Hynix retains a royalty-free perpetual license for their own internal use indefinitely.

Advantages: SK Hynix gets the first-mover advantage they need to outpace Samsung and Micron. ECSI gets a clear path to the broader market after the exclusivity period. The time-bound structure gives SK Hynix a strong incentive to commercialize quickly (use it or lose it).

Considerations: ECSI must negotiate a minimum commercialization commitment from SK Hynix to prevent them from shelving the technology during the exclusivity window. The clock on exclusivity should start from "first production tool qualified," not from JDA signing.

Option E — IP Split: Core vs. Joint Development IP

ECSI Risk: Low | SK Hynix Appeal: High *Ideal for: A true co-development partnership where both parties contribute significant engineering work*

When co-developing the production tool, new intellectual property will inevitably be created — specific automation mechanisms, fluid handling designs, control algorithms, wafer handling systems. This structure cleanly separates what each party owns.

- **Core IP (ECSI owns 100%):** The foundational CET patents — the conductive blanket mechanism, the boundary layer elimination physics, the electrochemical process itself.
- **Joint IP (SK Hynix and ECSI co-own):** New patents related to the machine design, automation, precision control systems, and 300mm wafer handling developed during the JDA.
- **License Terms:** SK Hynix receives a royalty-free license to ECSI's Core IP for their internal use. ECSI receives a royalty-free license to the Joint IP for all non-memory applications.

Advantages: Protects ECSI's foundational patents absolutely. SK Hynix has a strong incentive to contribute engineering resources because they co-own the resulting machine IP. Very fair and defensible structure.

Considerations: Requires careful IP assignment clauses in the JDA. Joint IP ownership can complicate future licensing to third parties (both parties must consent).

Option F — Equipment Vendor License (Lam Research / Applied Materials)

ECSI Risk: Medium | SK Hynix Appeal: Medium *Ideal for: SK Hynix wants production-scale tools built and maintained by their existing equipment partners*

SK Hynix is a chipmaker, not an equipment manufacturer. They will eventually want a company like Lam Research or Applied Materials to build, install, and maintain CET production tools at their fabs.

Structure: SK Hynix funds the R&D to prove the Alpha tool. Once proven, ECSI Fibrotools licenses the CET patents to SK Hynix's preferred equipment vendor (Lam Research, Applied Materials, or similar). The equipment vendor pays ECSI a royalty per machine sold or per wafer processed. SK Hynix receives a heavily discounted or royalty-free rate on the machines they buy — effectively giving them a return on their initial R&D investment.

Advantages: SK Hynix gets production-scale tools from a vendor they already trust and have service contracts with. ECSI gets a recurring royalty stream from every machine sold globally. This model scales far beyond SK Hynix alone.

Considerations: ECSI gives up direct control of the tool design and manufacturing. The equipment vendor may attempt to design around ECSI's patents once they understand the mechanism. Strong patent protection and licensing terms are critical.

Option G — Strategic Seed Investment

ECSI Risk: Medium | SK Hynix Appeal: Medium *Ideal for: If the JDA route stalls or SK Hynix prefers an equity relationship*

Rather than a JDA, SK Hynix's corporate venture arm makes a seed investment in ECSI Fibrotools in exchange for equity and options on exclusive licensing rights. ECSI uses the investment to hire engineers, build out the lab, and develop the Alpha tool independently. SK Hynix holds an option to acquire exclusive rights at a pre-agreed valuation once the Alpha tool is proven.

Advantages: ECSI retains operational independence. SK Hynix gets a financial stake and a strategic option without committing to a full JDA. This is a lower-commitment entry point for SK Hynix — easier to get approved internally.

Considerations: Equity dilution for ECSI. SK Hynix may not exercise their option if internal priorities shift. Seed investment amounts ($500K$–2M) are smaller than JDA funding, potentially slowing development.

PART 5: TARGET INTELLIGENCE — SK HYNIX PROFILE

Key People to Know

Name	Title	Relevance
Hoyoung Son	VP, Advanced Package Development	Primary technical champion for advanced packaging; directly responsible for HBM TSV and microbump processes
Cha Seon Yong	CTO	Sets the 30-year technology roadmap; ultimate authority on new process technology adoption
West Lafayette R&D Leads	Indiana Facility Team	Most accessible via the Purdue connection; on-the-ground decision-makers for the new facility
SRC Liaison Engineer	SK Hynix SRC Representative	Entry point via the Semiconductor Research Corporation pathway

Technology Roadmap & CET Relevance Windows

Timeframe	SK Hynix Milestone	CET Relevance
2025–2026	HBM4 production ramp; 300+ layer NAND	TSV aspect ratios increasing; copper fill uniformity is a yield limiter now
2027–2028	HBM5 development; West Lafayette facility online	Critical window — new facility needs new process tools; JDA should be signed by 2027
2029–2031	HBM5E, 3D DRAM, 400+ layer NAND	CET Alpha tool should be in pilot integration; exclusivity period begins
2032+	Post-exclusivity	ECSI licenses CET to broader market; SK Hynix retains royalty-free perpetual license

SK Hynix Collaboration Ecosystem

- **Open Research Platform (Global R&D24):** Formal program for external R&D partnerships — submit proposals at research.skhynix.com
- **Applied Materials EPIC Center Partnership:** $5B co-innovation agreement signed March 2026; SK Hynix is actively co-developing next-gen process tools with equipment vendors
- **Purdue Research Park Facility:** $3.87B investment; R&D operations beginning 2026–2028; Birck Nanotechnology Center is the natural neutral ground for joint work
- **CHIPS Act Commitments:** SK Hynix received U.S. government incentives tied to domestic R&D collaboration; a joint ECSI–SK Hynix CHIPS grant proposal aligns with their federal obligations
- **SRC Membership:** SK Hynix co-funds pre-competitive university research through the SRC; Purdue is an SRC member institution

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PART 6: 30-DAY ACTION ITEMS

The following eight actions should be completed within the next 30 days to initiate the engagement.

Action 1 — Brief the Purdue Champion (Week 1) Schedule a call. Be fully honest about CET's current stage. Provide the Technology Vision Brief. Ask them to identify the right SK Hynix technical contacts at the West Lafayette facility and to make a direct email introduction.

Action 2 — Draft the Technology Vision Brief (Week 1–2) Write the 2-page document. It must look like an academic white paper. Include: CET physics overview, benchtop proof-of-concept data (including the 100µm setback framed correctly), a diagram of the CET sandwich structure, and a clear co-development proposal with a call to action.

Action 3 — Prepare the "Setback Data" Slide (Week 2) Package the 100µm platinum over-plating data into a single compelling slide. The narrative: "The deposition engine is incredibly powerful. We need your help to build the precision control system." This slide should be ready before any SK Hynix meeting.

Action 4 — Submit to SK Hynix Open Research Platform (Week 2) Visit research.skhynix.com/open_research_platform and submit a formal research collaboration proposal for "CET-Based TSV Filling for Advanced HBM Packaging." This creates a second, independent point of contact inside SK Hynix's R&D organization.

Action 5 — Draft the Mutual NDA (Week 2) Have a standard mutual NDA template ready before any technical meeting. Do not wait until after a meeting is scheduled — have it ready to

send the moment a meeting is confirmed.

Action 6 — Research the West Lafayette Team (Week 2–3) Use LinkedIn, ECTC/IMAPS conference proceedings, and Purdue's semiconductor faculty directory to identify specific SK Hynix R&D engineers at the West Lafayette facility who work on TSV and advanced packaging. Know their names and their published work before the first meeting.

Action 7 — Contact Purdue Birck Nanotechnology Center (Week 3) Reach out to Birck's industry partnership office. Understand the process for hosting a joint industry R&D project. Confirm that the first CET feasibility test can be conducted at Birck using their metrology equipment.

Action 8 — Register for ECTC or IMAPS (Week 3–4) Identify the next upcoming ECTC or IMAPS conference. Register to attend. Submit an abstract if the deadline allows. These conferences are where SK Hynix process engineers go to learn about new technology — being present is not optional.

PART 7: CULTURAL INTELLIGENCE — ENGAGING A KOREAN CHAEBOL

These five principles are non-negotiable when engaging SK Hynix.

1. Relationship Before Business Korean corporate culture is relationship-first. The Purdue introduction is not a shortcut — it is the only acceptable entry point. Never cold-contact SK Hynix directly. Every communication should reinforce the relationship, not just advance the transaction.

2. Hierarchy Is Sacred Always address the most senior person in the room first. When presenting, direct your key messages to the highest-ranking person present, even if the technical questions come from junior engineers. Never contradict or embarrass a senior person in front of their team.

3. Patience Is Respect Expect 6–12 months from first contact to a signed JDA. Do not interpret silence as rejection. Follow up gently and consistently. Pushing too hard signals desperation and disrespect for their process.

4. Data Over Claims Korean semiconductor engineers are among the most technically rigorous in the world. Every claim must be backed by reproducible data. Do not make performance claims you cannot immediately support with a graph or a cross-section image. The 100µm setback, presented with full data, will earn more respect than a polished marketing claim.

5. The Long Game SK Hynix thinks in 10-year technology roadmaps. Frame CET not as a solution for today's problem, but as the foundational technology for their 2029–2031 HBM5 and

3D DRAM roadmap. The longer the time horizon you can credibly address, the more strategic — and therefore more fundable — the partnership becomes.

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